Physics of Metal-Oxide-Semiconductor (MOS) Structures (Part I)

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Overview

1) MOS structures in important semiconductor device classes

2) Physics of MOS - Structures
Overview of MOS structures in important device applications

Logic devices: Metal - Oxide Semiconductor Field Effect Transistor

Besides isolation (see image) of the individual transistors from each other, thermally grown silicon dioxide (SiO$_2$) plays a crucial role in the performance of the transistor as the gate dielectric layer.

transistor physics and the role of dielectrics will be discussed in the lectures held on 12/2/2005
Overview of MOS structures in important device applications

Volatile Memory devices: Dynamic random access memory (DRAM)

Yesterday:
planar cells

Today:
3D cells

Dielectrics play a crucial role to guarantee the storage of sufficient charge despite continuously shrinking device dimensions

\[ |Q_s| = C_s V_{cc} = A \frac{\varepsilon_i}{d} V_{cc} \]

Volatile memories and the role of dielectrics will be discussed in the lectures held on 12 / 9 / 2005
Nonvolatile Memory devices: Flotox and Flash Concepts

Today’s market leader:

![Diagram showing charge injection and driven out by high voltage pulses](image)

Charge is injected (write) and driven out (erase) by high voltage pulses

\[ \Delta V_T = -\frac{Q_S}{C_{CG}} \]

Nonvolatile memories and the role of dielectrics will be discussed in the lectures held on 12 / 16 / 2005
Overview of MOS structures in important device applications

Nonvolatile Memory devices: Ferroelectric random access memory (Fe-RAM)

Today and more to come in future:

Ferroelectrics allow to store information when the power is switched off

Volatile memories and the role of dielectrics will be discussed in the lectures held on 12 / 16 / 2005
Overview of MOS structures in important device applications

Scaling makes the development of advanced dielectric layers a „hot topic“ in materials research

Ongoing scaling requires to thin out the dielectric layer

Dielectric layers need to meet very different requirements specific for each application

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<th>REQUIREMENTS</th>
<th>Standard CMOS</th>
<th>Nonvolatile Memories</th>
<th>FLOTOX</th>
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<td>High Mobility for High Speed</td>
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<td>High Reliability against Hot Carriers injected from substrate</td>
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<td>Low Leakage &amp; Few Dielectrics Breakdowns</td>
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<tr>
<td>High Reliability against Carriers flowing through films (high QBD, etc.)</td>
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<td>Vital</td>
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Gate Dielectrics in Active FETs used as Passive Elements
Overview

1) MOS structures in important semiconductor device classes

2) Physics of MOS - Structures
Ideal MOS - Structure

Very simple system geometry ….. but quite complicate physics

Let's start with some idealizations:

1) Work function difference is zero

\[ \phi_{ms} \equiv \phi_m - \left( \frac{x + E_g}{2q} + \phi_F \right) = 0 \]

\[ \phi_F = - \phi_i \ln \left( \frac{N_D}{n_i} \right) \] for n-type

\[ \phi_F = \phi_i \ln \left( \frac{N_A}{n_i} \right) \] for p-type

2) No charged defects in the insulator

3) No current over the dielectric (perfect insulator)
If you bias the metal gate at different gate voltages $V_G$, three different situations can in principle arise:
(discussion is based here on p-type Si)

**Accumulation:**
majority carriers accumulate in semiconductor surface region

**Depletion:**
negative charge appears in semiconductor surface region
because majority carriers are chased away
(uncompensated acceptor atoms rest behind)
and minority carriers are attracted

**Inversion:**
high negative charge is induced in semiconductor surface region
more minority than majority carriers
($E_i$ crosses over $E_F$ in surface region (intrinsic condition) )
Derive a relationship between the charge in the semiconductor and the surface band bending

Band bending:
zero inside the semiconductor;

Surface potential:
referenced to Fermi – potential

Result:
Band bending is the sum of surface plus Fermi potential

Using the band bending (or surface potential) as a function of the distance $x$ from the interface, the charge carrier concentration can be described as a function of $x$:

For specific doping level $N_A$ and $N_D$

$$p(x) = N_A e^{-\psi/\phi_i} = n_i e^{-\phi/\phi_i}$$

$$n(x) = N_D e^{\psi/\phi_i} = n_i e^{\phi/\phi_i}$$

intrinsic carrier concentration
Derive a relationship between the charge in the semiconductor and the surface band bending

From these relations, the 1D Poisson equation is solved under the following assumptions:

1) $N_A$ is uniform over $x$; 2) Boltzmann statistics; 3) no surface charge quantization

$$\frac{\partial^2 \psi}{\partial x^2} = \frac{-\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s} \left[ (p(x)-n(x))+N_D-N_A \right]$$

First Integration:
Electric field is given by potential gradient

$$\int_0^\psi \frac{\partial \psi}{\partial x} d\left( \frac{\partial \psi}{\partial x} \right) = -\frac{q}{\varepsilon_s} \int_0^\psi \left[ N_A (e^{-\phi_t/\phi} - 1) - N_D (e^{\phi_t/\phi} - 1) \right] d\psi$$

$$\varepsilon \equiv -\frac{\partial \psi}{\partial x} = \pm \sqrt{2} \frac{\phi_t}{L_D} F(\psi, N_A) \quad L_D = \sqrt{\frac{\varepsilon_s \phi_t}{qN_A}}$$

$$F(\psi, N_A) = \sqrt{e^{-\psi/\phi_t} + \psi/\phi_t - 1 + (n_i/N_A)^2 (e^{\psi/\phi_t} - \psi/\phi_t - 1)}$$

1D Poisson equation:
non-uniform volume charge density causes curvature of potential

Debye Length

just for completeness
Derive a relationship between the charge in the semiconductor and the surface band bending

The relationship between the charge in the semiconductor surface and the surface band bending then reads:

$$Q_s \equiv -\varepsilon_s \varepsilon_r = \mp \sqrt{2} \frac{\varepsilon_s \phi_t}{L_D} F(\psi_s, N_A)$$

Influences of doping concentration:
1) certainly, Fermi level is a function of doping
2) the more p-type the wafer, the higher the potential for inversion

Accumulation:
From the sign of surface band bending:
semiconductor charge is positive

Depletion:
From the sign of surface band bending:
semiconductor charge is negative

Inversion:
From the sign of surface band bending:
semiconductor charge is negative

(a) $L = 100$ nm Transistor; (b) $L = 10$ nm Transistor:
dielectrics has to survive higher electric fields

Solid Line: $N_A = 4 \times 10^{15}$ cm$^{-3}$; Dotted Line: $N_A = 2 \times 10^{17}$ cm$^{-3}$