Physics of Metal-Oxide-Semiconductor Structures (Part II)

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Overview

1) C-V measurements to characterize ideal MOS - Structures

2) C-V measurements to characterize non - ideal MOS - Structures
A relationship between the charge in the semiconductor and the surface band bending

The relationship between the charge in the semiconductor surface and the surface band bending was derived last week:

\[ Q_s \equiv -\varepsilon_s \varepsilon_s = \mp \sqrt{2} \frac{\varepsilon_s}{L_D} \phi_t F(\psi_s, N_A) \]

Influences of doping concentration:
1) certainly, Fermi level is a function of doping
2) the more p-type the wafer, the higher the potential for inversion

Accumulation:
From the sign of surface band bending:
semiconductor charge is positive

Depletion:
From the sign of surface band bending:
semiconductor charge is negative

Inversion:
From the sign of surface band bending:
semiconductor charge is negative

(a) L = 100 nm Transistor; (b) L = 10 nm Transistor:
dielectrics has to survive higher electric fields

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(a) L = 100 nm Transistor; (b) L = 10 nm Transistor:
dielectrics has to survive higher electric fields
What is measured is not the charge in the semiconductor as a function of band bending but the differential capacitance as a function of applied voltage:

The differential capacitance is measured by carrying out a voltage sweep on a MOS structure with a constant ramp (e.g. +4 to -4 V) while a small AC voltage (e.g. 25 mV) of a certain frequency (e.g. 100 KHz) is superimposed.
The measured differential capacitance is nothing else than the change of the semiconductor surface charge as a function of the changing band bending when the applied potential is varied.

\[
C_s = \frac{\partial Q_s}{\partial \psi_s} = \frac{\varepsilon_s}{\sqrt{2L_D}} \left| 1 - e^{-\psi_s/\phi_t} + \left( \frac{n_i}{N_A} \right)^2 \left( e^{\psi_s/\phi_t} - 1 \right) \right| F(\psi_s, N_A)
\]

For example, when the applied potential makes the bands flat, we get:

\[
c_s (\text{flat-band}) = \lim_{\psi_s \to 0} C_s = \frac{\varepsilon_s}{L_D}
\]

In this way, if the semiconductor dielectric constant is known, the Debye length can be measured.
A view on the MOS – structure under inversion

Charge neutrality:

\[-Q_G = Q_S = Q_I + Q_D = Q_I - qN_A w\]

Displacement Continuity:

\[\varepsilon_i \varepsilon_i = \varepsilon_s \varepsilon_s\]

Potential Drop:

\[V_G = \psi_s + V_i\]

The potential drop over the oxide is given by:

\[V_i = \varepsilon_i d = -Q_s / C_i\]

We see: system is series combination of insulator and semiconductor capacitance, so that total C is given by:

\[C = \frac{1}{1/C_i + 1/C_s}\]

\[C_i : \text{constant regardless of } V_G\]

\[C_s : \text{varies strongly with } V_G\]
A typical C-V characteristics of an ideal MOS – structure

The system is a series combination of insulator and semiconductor capacitance:

$$C = \frac{1}{1/C_i + 1/C_s}$$

Insulator capacitance:

Curve a: low frequency C-V measurement (minority carriers can follow the AC voltage)

Under inversion, the exponential dependence of the minority carrier concentration on the surface band bending results in high semiconductor charge so that insulator capacitance is measured.

But a word about the minority carriers:

Exchange of minority carrier generation between the bulk with the semiconductor surface region has a certain time constant.
High frequency C-V characteristics of an ideal MOS – structure

The system is a series combination of insulator and semiconductor capacitance:

\[ C = \frac{1}{1/C_i + 1/C_s} \]

**Insulator capacitance:**

\[ C_{FB} (\psi_s = 0) \]

**Curve b:** high frequency C-V measurement (minority carriers can not follow the AC voltage)

If AC-frequency is higher, inversion layer charge does not follow the modulation anymore.
High frequency C-V characteristics of an ideal MOS – structure

The system is a series combination of insulator and semiconductor capacitance:

\[ C = \frac{1}{1/C_i + 1/C_s} \]

Insulator capacitance:

Curvature b: high frequency C-V measurement (minority carriers can not follow the AC voltage)

The minority carriers are generated with a time constant given by \( RC \).

If frequency is too high, the semiconductor charge follows the AC variation by varying the width of the semiconductor depletion region.
High frequency C-V characteristics of an ideal MOS - structure

The system is a series combination of insulator and semiconductor capacitance:

\[ C = \frac{1}{1/C_i + 1/C_s} \]

**Insulator capacitance:**

Curve b: high frequency C-V measurement (minority carriers can not follow the AC voltage)

A square root dependence exists between the depletion charge and the band bending so that the differential capacitance of the semiconductor is here far lower than in case of the low-frequency measurement.

**Depletion approximation**

\[ W_m = \sqrt{\frac{2 \epsilon_s \cdot 2 \phi_F}{qN_A}} = 2 \sqrt{\frac{\phi_F}{\phi_t}} L_D \]

\[ V_T = 2\phi_F + \frac{\sqrt{2 \epsilon_s qN_A \cdot 2 \phi_F}}{C_i} \]
The system is a series combination of insulator and semiconductor capacitance:

\[ C = \frac{1}{1/C_i + 1/C_s} \]

Insulator capacitance:

Curve b: high frequency C-V measurement (minority carriers can not follow the AC voltage)

Depletion approximation

\[ C_s = \frac{\varepsilon_s}{\sqrt{2L_D}} \left| 1 - e^{-\psi_s/\phi_t} \right| F'(\psi_s) \]

\[ F'(\psi) = \sqrt{e^{-\psi/\phi_t} + \psi/\phi_t - 1} \]

e.g. semiconductor doping can be extracted in depletion region
Non-equilibrium C-V characteristics of an ideal MOS – structure

The system is a series combination of insulator and semiconductor capacitance:

\[ C = \frac{1}{\frac{1}{C_i} + \frac{1}{C_s}} \]

Insulator capacitance:

\[ C_{FB} (\psi_s = 0) \]

Curve c: non-equilibrium C-V measurement (deep depletion)

- Insulator capacitance:
  \[ C = \frac{1}{d/\varepsilon_i + L_D/\varepsilon_s} \]
- Semiconductor capacitance:
  \[ C = \frac{1}{d/\varepsilon_i + W/\varepsilon_s} \]

- Depletion region exceeds steady state width \( w_m \)

\[ |Q_s| = \sqrt{2} \frac{\varepsilon_s \phi_t}{L_D} F'(\psi_s) \]

\[ F'(\psi) = \sqrt{\frac{e^{-\psi/\phi_t}}{\psi/\phi_t - 1}} \]

Vary \( V_G \) more rapidly than minority carrier response time

Inversion layer is not formed

Depletion region exceeds steady state width \( w_m \)
Overview

1) C-V measurements to characterize ideal MOS - Structures

2) C-V measurements to characterize non-ideal MOS - Structures
Non-ideal behavior: 1) Work Function Difference

In general, the work function of the gate electrode and the Si substrate are different:

\[
\phi_{ms} = \phi_m - \left[ \left( x + \frac{E_g}{q} \right) - \frac{E_i - E_v}{q} + \phi_F \right]
\]

Work function adjustment by varying Si substrate doping
Non-ideal behavior: 2) Charges

Namely four different charge species are distinguished in MOS structures:
Non-ideal behavior: Example of fixed charge in the insulator

The effect of trapped charge in the insulator is to screen a part of the applied field $V$:

**Band diagramm:**

**C – V curve**

**Quantification:**

$$\Delta V = - \frac{q}{\varepsilon_i} \int_0^d (d - x) n_{ot}(x) \, dx$$

Trapped charge is most serious when located at insulator / silicon interface ($x = 0$)

Trapped charge is not effective when located at Insulator / metal interface ($x = d$)
Non-ideal behavior: Example of interface states

**Interface states:**
energy levels which are distributed over the band gap and can be charged and discharged by a varying potential

Above midgap: acceptor-like
(negative when filled and neutral when empty)

Below midgap: donor-like
(neutral when filled and positive when empty)

**C-V curves:**
Interface states distort C-V curves
Negative shift due to donor IF states (positive)
Positive shift due to acceptor IF states (negative)
Non-ideal behavior: 3) Current transport through the insulator

Different mechanisms exist which can be identified by

a) plotting the measured J-V characteristics in the right way (e.g. Fowler Nordheim plot: J/E against 1/E))

b) measuring the J-V characteristics for changing parameters (e.g. temperature)

<table>
<thead>
<tr>
<th>Mechanism</th>
<th>Equation</th>
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<tbody>
<tr>
<td>Fowler-Nordheim Tunneling</td>
<td>( J = \frac{A}{4\phi_0} \frac{1}{E_i} \exp\left(-\frac{2B \phi_0^{3/2}}{3E_i}\right) )</td>
</tr>
<tr>
<td>Direct Tunneling</td>
<td>( J = \frac{A}{d^2} \left( \frac{V_2}{2} \right)^2 \exp\left(-Bd \sqrt{\phi_0 - \frac{V}{2}} \right) )</td>
</tr>
<tr>
<td>Schottky Emission</td>
<td>( J \propto T^2 \exp\left(-\frac{\phi_0 - \sqrt{E_i} / C}{\phi_i}\right) )</td>
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<tr>
<td>Poole-Frenkel Emission</td>
<td>( J = E_i \exp\left(-\frac{\phi_0 - 2\sqrt{E_i} / C}{\phi_i}\right) )</td>
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<tr>
<td>Hopping (Ohmic) Conduction</td>
<td>( J \propto E_i \exp\left(-\frac{\Delta E_{el}}{kT}\right) )</td>
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